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Fabrication of PZT actuated cantilevers on silicon-on-insulator wafers for a RF microswitch

Hong Wen Jiang*, Paul Kirby* and Qi Zhang
Nanotechnology and Microsystems Group, School of Industry and Manufactures, Cranfield University, UK.

ABSTRACT

A processing scheme for fabricating $Pb(Zr_xTi_{1-x})O_3$ thin film actuated silicon cantilevers using silicon-on-insulator wafers is described. Such piezoelectrically actuated cantilevers are being investigated for RF microswitches. The microswitch design specification requires the $Pb(Zr_xTi_{1-x})O_3$ thin film to be at least 1μm thick to achieve the adequate deflection at an operating voltage of 10V. A two-stage dry-wet etching process was developed to reliably pattern the 1μm $Pb(Zr_xTi_{1-x})O_3$ film. To release the $Pb(Zr_xTi_{1-x})O_3$ cantilevers on silicon-on-insulator wafers it is necessary to perform deep silicon etching from both sides of the wafer. The $Pb(Zr_xTi_{1-x})O_3$ thin film was prepared by sol-gel method. The piezoelectric coefficient d_{31} was calculated as 14pC/N.

Keywords: PZT thin film, MEMS, RF switch, SOI, RIE, DRIE, BOE, micromachining, cantilever

1. INTRODUCTION

Microelectromechanical systems (MEMS) structures are being investigated and developed as possible RF components. Their applicability arises because the dimensions of MEMS structures are comparable to those of on-wafer planar transmission line structures. The signal conductor in a coplanar transmission line usually has a width of several hundred microns, typical of the dimensions of MEMS structures. Examples of MEMS RF components are microswitches and suspended transmission line structures that can give improved filter performance. These components could find wide application if robust devices could be fabricated.

The silicon based microswitch is one of the mostly developed RF MEMS devices. Compared to the performance of traditional semiconductor switches MEMS switches have achieved lower insertion losses when closed and higher isolation when open. Most of the microswitches that have been developed to date use electrostatic actuation to achieve a switching gap of between 3 μm and 4 μm [1~4] requiring an operating voltages between 20 volts and 100 volts. However, high DC voltages are not usually available in microwave circuits.

The work reported here is part of a project investigating possible RF and microwave components using silicon MEMS structures that incorporate piezoelectric thin film. Such an investigation requires the development of fabrication techniques for accurately incorporating piezoelectric film and the availability of processes for fabricating silicon microstructures. The latter process must be compatible with the presence of the piezoelectric thin film.

In terms of material properties $Pb(Zr_xTi_{1-x})O_3$ (PZT) is the piezoelectric material of choice for actuation because of its powerful electromechanical conversion. If the integration of PZT thin films can be successfully achieved then high force-displacement actuation at low drive voltages will become a design option for RF and microwave MEMS components. Ideally, piezoelectric materials would be able to be used in a form compatible with MEMS processing. The fabrication process described here allows the incorporation of PZT thin films up to 1μm thickness onto a silicon microcantilever for application as a microwave switch. Using piezoelectric actuation in RF switches is one possible way to have low operating voltages. In a previous paper [5] we showed that a 10μm switching gap could be achieved by a 1μm thick PZT film on a 203μm×176μm×2μm cantilever with a sustaining voltage of 10V.

* h.w.jiang@cranfield.ac.uk; phone 044 1234 750111 ext. 2422; fax 044 1234 754067
* p.b.kirby@cranfield.ac.uk; phone 044 1234 751346 fax 044 1234 754067

The use of silicon-on-insulator (SOI) wafers has simplified the processing of many MEMS structure or devices. Accelerometers, gyroscopes and optical devices have been fabricated on SOI substrates. In this paper we present in detail a process for fabricating PZT actuated cantilevers.

2. FABRICATION PROCESS

The realization of a PZT cantilever involved the development of two components: the PZT actuating element and the silicon cantilever. Firstly processes were developed for integrating PZT onto the device layer of a SOI wafer. The PZT processing was completed before any deep etching of the silicon wafer took place as PZT processing on a flat silicon surface was more straightforward. The actuating element is a PZT stack consisting of a patterned PZT layer sandwiched between patterned top and bottom electrodes. If the top electrode, PZT and bottom electrode were patterned in one process step there would be the possibility of metal shorting between the top and bottom electrodes. For this reason the layers that make up the PZT stack were recessed with respect to each other as shown within the circle in Figure 1.

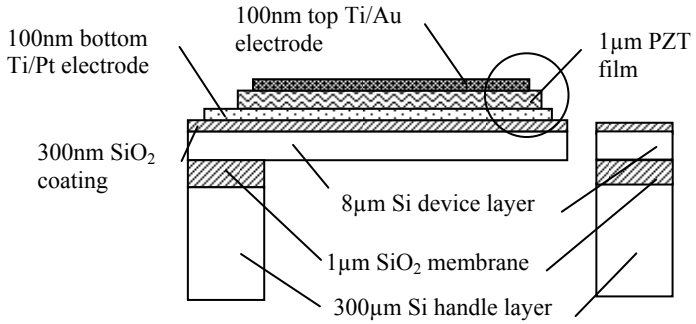

Figure 1: Schematic show of the PZT cantilever

The second stage of the process was to make the silicon cantilever on which the PZT stacks were located. The cantilever fabrication process involved Deep Reactive Ion Etching (DRIE) to the buried oxide layer first from the front and then from the back of the SOI wafer. In previous work cantilevers and beams have been produced by lateral sacrificial, HF, etching of the buried oxide layer after front side silicon etching to this layer. This was not possible here as it was very difficult to protect the PZT layers during HF etching. Figure 1 shows schematically the PZT cantilever processed from a SOI wafer.

The processing scheme used is sketched in Figure 2 (a ~ f). A SiO_2 layer was incorporated on top of the SOI wafer to act as a barrier layer against lead diffusion during PZT deposition (Figure 2a). The PZT thin film was deposited by the sol-gel method on top of a Ti/Pt (8nm/100nm) bottom electrode. It is difficult to produce high quality PZT on top of a patterned Pt electrode so the etching of the bottom Pt electrode was the last process in the stack fabrication (Figure 2c). The Ti/Au (8nm/100nm) top electrode was produced using a lift-off bi-layer resist process (Figure 2a). Lift-off is a more straightforward process for fabricating patterned electrodes on top of PZT than dry etching. The PZT film was patterned by two-stage process, reactive ion etching (RIE) and wet chemical etching (Figure 2b). All electrodes were sputter deposited. The patterning of the Ti/Pt bottom electrode (Figure 2c) was also performed by a RIE process: 30 minutes 120W etch in an Ar gas plasma.

The front side silicon etching to the buried oxide layer was performed before the back side silicon etching. In this order it was not necessary to attempt processing resist on top of a thin silicon membrane. To access the silicon device layer for etching it was necessary to etch through the SiO_2 barrier layer (Figure 2d). A HF buffered oxide etch (BOE) was used to etch this oxide layer. The same photoresist mask used for the BOE process also provided the mask for the DRIE (Figure 2e) of the SOI device layer. Following the back side silicon etching (Figure 2f) the cantilevers were released by removing the buried SiO_2 membrane around the cantilever using a CHF_3/O_2 RIE process as shown in Figure 1.

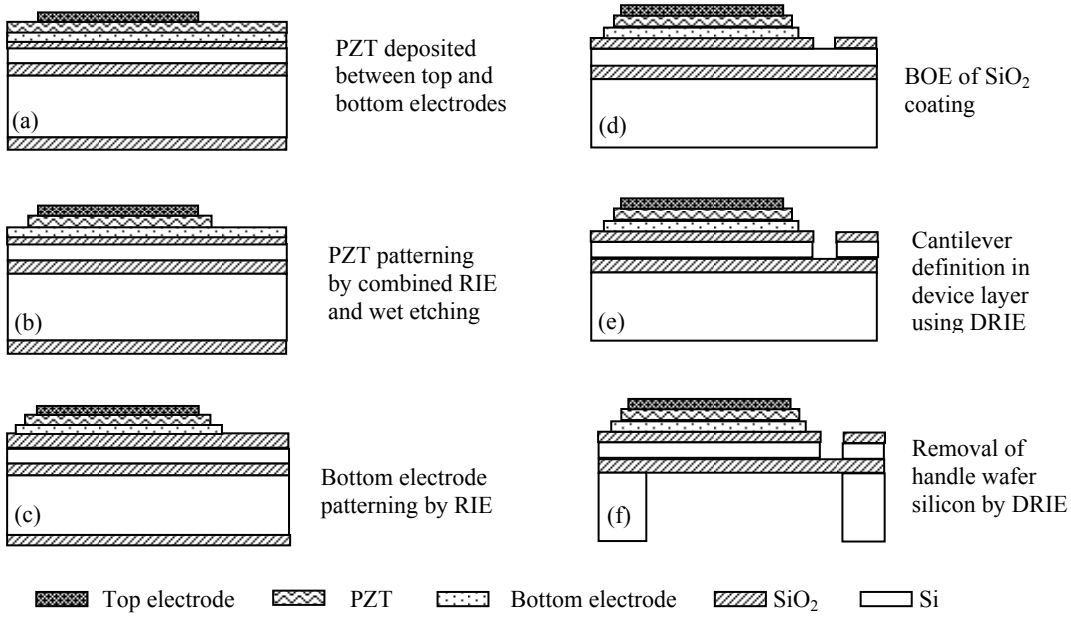

Figure 2: Fabrication process flow diagram

3. PROCESS RESULTS AND DISCUSSIONS

3.1. PZT patterning

Etching trials indicated that for features above 100µm wet etching could give satisfactory pattern definition. For features below 50µm dry etching technique was necessary to provide a sufficient accuracy. However, to date no dry etching process with a high reactive component has been found, and for thicker PZT films (≥ 1µm) dry etching time can be several hours which were demanding for the survivability of the masking material.

A 1µm PZT film that was wet etched with HF(0.9%)/HCL(8.2%)/H_2O(90.9%) and HNO_3(50%)/H_2O(50%) solutions is shown in Figure 3 (a), the ragged edge has a definition between 5µm and 8µm. In contrast Figure 3 (b) shows a 2µm edge definition produced by RIE

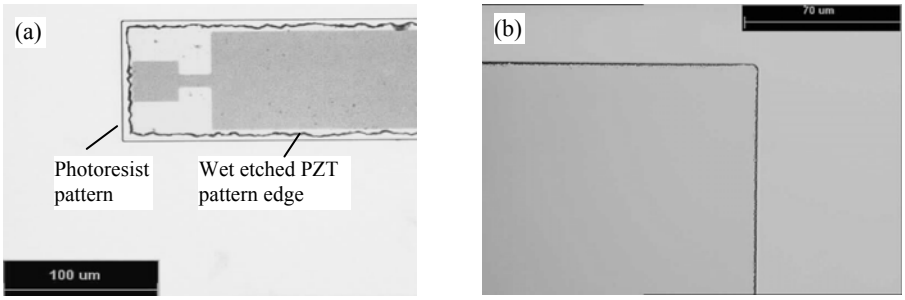

Figure 3: PZT pattern produced by wet etching (a) and the reactive ion etching (b)

During RIE of PZT it was found that the RF power level and the thermal contact between the wafer and the wafer stage were important factors in determining whether damage to the resist took place. Figure 4(a) and (b) shows that at an RF power of 200W damage to the photoresist was reproduced on the surface of the PZT. However, at 175W the PZT surface remained free of damage (Figure 4c), although the edges of the PZT pattern were rounded with slight damage at the periphery. The use of vacuum grease to improve the thermal contact between the wafer and the chamber sample

stage eliminated any degradation to the photoresist as shown in Figure 5(a). The Figure shows a PZT pattern covered by the undamaged photoresist after 3hours of a RIE process at a power of 150W and a pressure of 38mTorr.

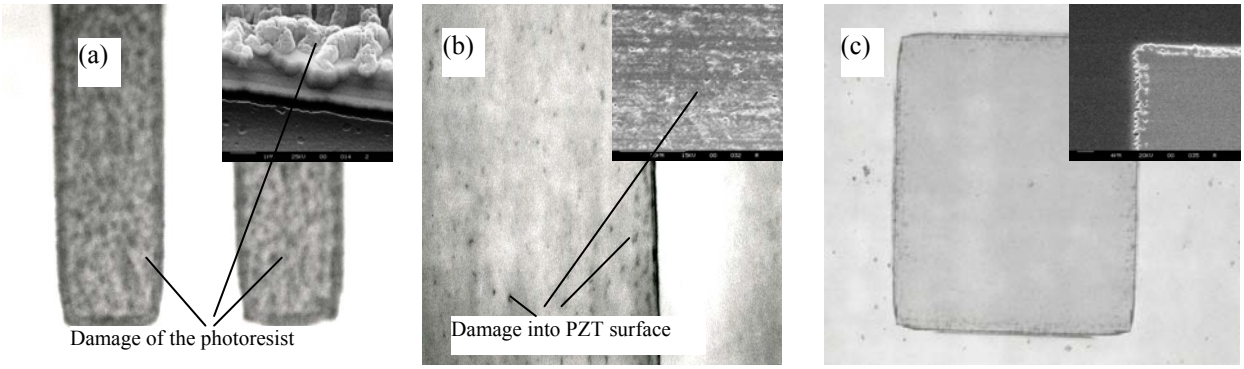

Figure 4: PZT pattern processed at RF power of 200W and 175W (the inner graphs are the SEM images)
(a) damaged photoresist; (b) the damage deepened into the PZT surface; (c) undamaged PZT surface

Dry etching was stopped before reaching the bottom Pt electrode as the photoresist mask was then easier to remove. The remaining PZT layer was then removed by wet etching. This two stage etch has the advantages that no over etching into underlying Pt occurred and results in a cleanly etched surface. Figure 5(b) shows the PZT patterns that were processed by this two stage process.

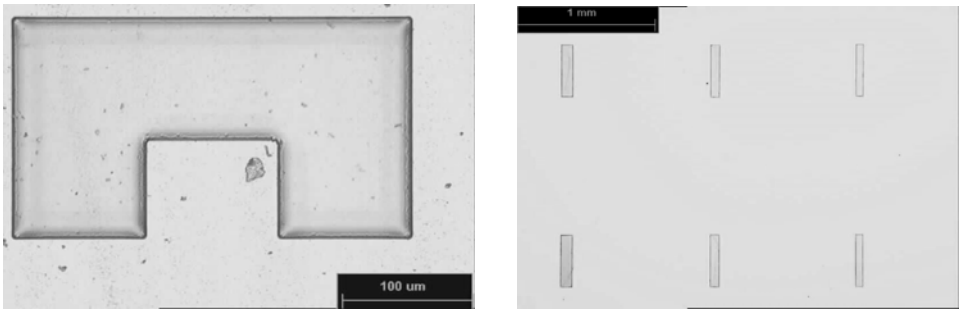

Figure 5: (a) Undamaged photoresist pattern on PZT following dry etching, (b) PZT array processed using the two stage process

Figure 6 shows a SEM image of a PZT stack processed as above described. The Figure also reveals how the top electrode is recessed relative to the PZT and similarly the PZT with respect to the bottom electrode.

3.2. DRIE process

3.2.1 PZT encapsulation

The PZT was encapsulated with a photoresist layer during the deep etching of silicon. The same encapsulation layer also protected the PZT during buffered HF etching of the top surface oxide (Figure 2e). This oxide layer was etched to expose the silicon surface ready for DRIE. An opening in the Pt and PZT has already been made at this stage so the photoresist encapsulant was arranged to overlap the PZT edge at the opening so that no lateral etching occurs during the HF BOE process.

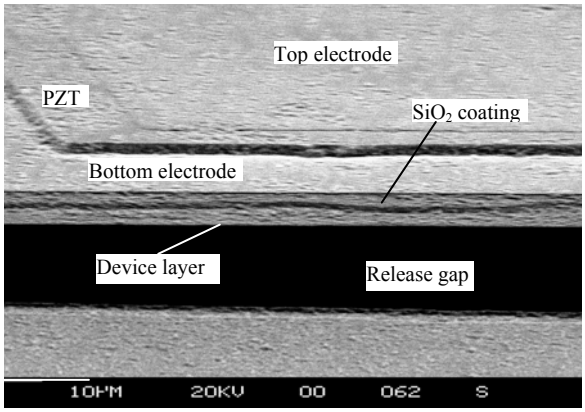

Figure 6: PZT stack on top of silicon cantilever

The encapsulant also served to reduce the risk of contamination of the etching chamber by PZT components. A 1.8µm thick hard-baked positive photoresist provided sufficient protection for both processes. Silicon etching was performed using the anisotropic process patented by Franz Laermer and Andrea Schilp [6] in a Multiple ICP reactor manufactured by Surface Technology Systems (STS). An illustration of the process is shown in Figure 7(a). As a comparison Figure 7(b) shows a poor edge definition if the resist is not hard baked.

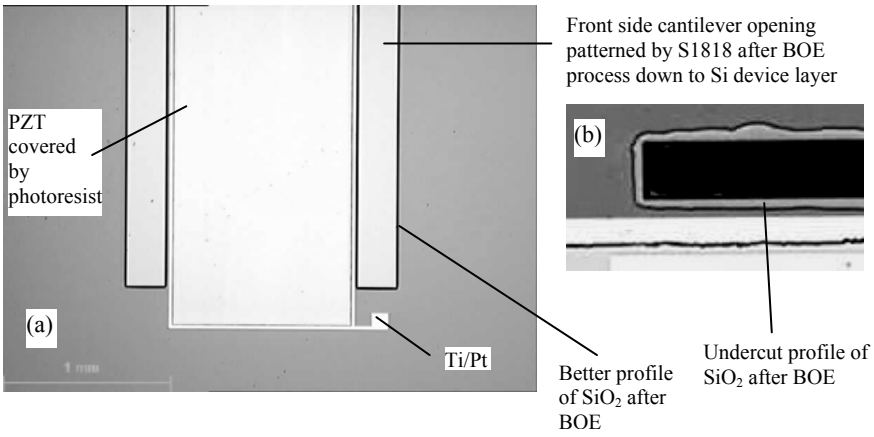

Figure 7: (a) Cantilever with PZT/Ti/Pt on top shows the PZT was covered fully by the photoresist, (b) Poor edge definition after BOE process in which the photoresist was not hard baked

3.2.2 Etching of silicon to fabricate cantilevers

As previously described the fabrication of silicon cantilevers using a SOI wafer involved a shallow front side followed by a deep back-side etch. In both cases the process finished on the buried oxide layer. It was only the silicon in the device layer part of the SOI wafer that formed the cantilever; the handle wafer being completely removed from below the cantilever. The precision of the front surface etch was therefore important in determining the mass and shape of the cantilever. For this reason short period passivation and etching cycles were used in order to reduce the depth of 'scalloping' during the DRIE process. Etching trials revealed that a smoother etch surface was produced with the low operating pressure resulting from a low setting of automatic pressure control (APC) valve. Figure 8(a) reveals a smooth surface for a setting of 55° compared to a rougher surface (b) for an APC setting of 72°. For the deeper backside silicon etch a more anisotropic profile was obtained with a higher working pressure in the chamber. Figure 9 shows the etching results of handle layer (a) and device layer (b).

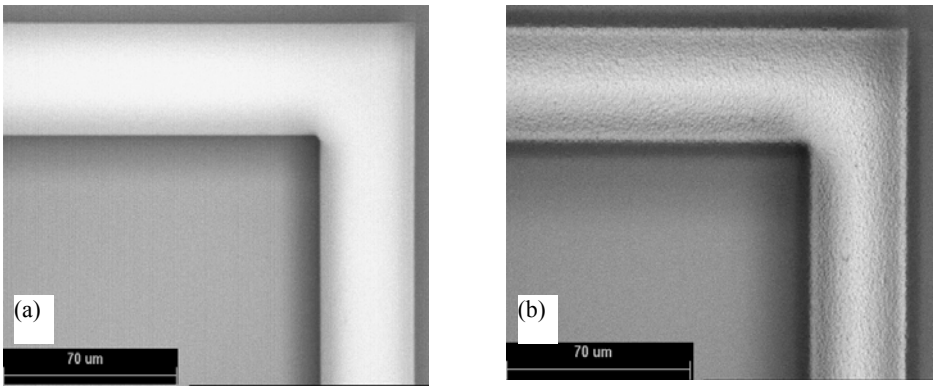

Figure 8: (a) Smooth surface obtained following DRIE using low pressure, (b) Rougher surface obtained at higher pressure

3.2.3 Use of a backing wafer during DRIE

As the silicon etch-front approaches the buried oxide layer during the back side process, the possibility of breaking sample and the buried oxide layer can cause the release of Helium gas and contamination of the chamber. This required the use of a silicon supporting wafer attached to the front-side surface of the cantilever wafer. The method of attachment must provide good thermal contact to the helium cooled chuck otherwise the resist mask will be damaged during the long back side process (>150mins).

We used 'cool grease' as the adhesion layer. A uniform thin layer was applied by heating the wafer to between 90°C ~ 100°C which allowed the grease to be applied smoothly. At the end of the etching process the grease was easily removed by dissolution of acetone. Vacuum grease can also be used and this dissolves readily in IPA.

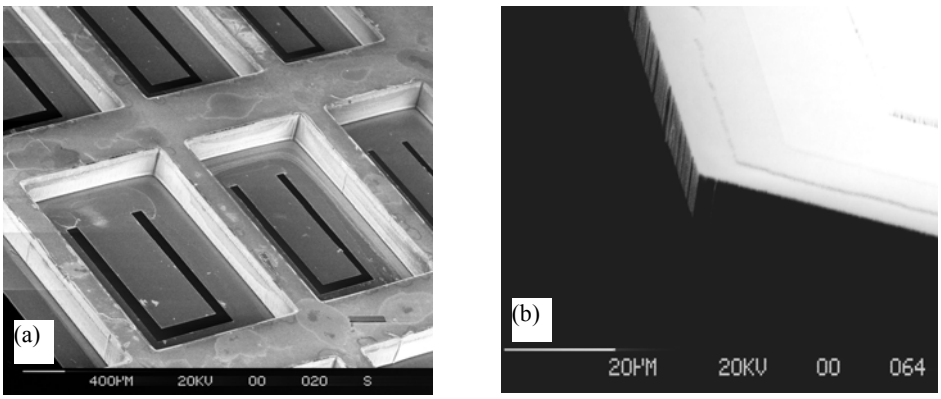

Figure 9: DRIE of handle layer down to SiO_2 membrane

3.2.4 Cantilever bending after final release

Bending caused by residual stress is an important issue for MEMS cantilever structures. The stresses in the layers on the silicon cantilevers are determined by the deposition processes used to produce the layers.

To identify the stress state of the layers that made up the cantilever wafer curvature measurements were performed using a profiler. Under the deposition conditions used the stress in the PZT layer was balanced by the other layers that made up the PZT stack and relatively flat cantilevers were obtained as shown in Figure 10.

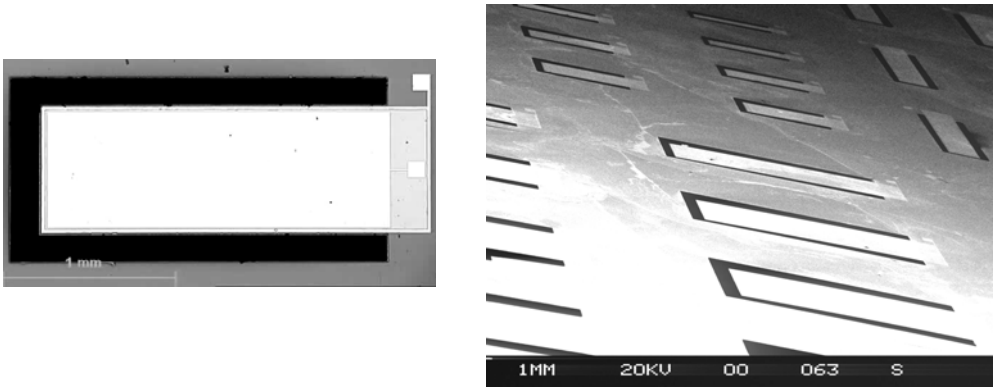

Figure 10: Flat PZT cantilever after the final release process

4. ELECTRICAL AND PIEZOELECTRIC PROPERTY MEASUREMENT

4.1.X-Ray Diffraction analysis

The orientation and phase purity of the PZT thin film was characterized by XRD method using a Siemens D5005 diffractometer. The XRD spectrum in Figure 12 shows that the PZT thin film used here was highly [111] orientated.

4.2. Dielectric constant (ε_r), dielectric loss (tan δ) and piezoelectric constant (d_{31})

Figure 13 shows the dielectric properties of the PZT thin film. The dielectric constant, ε_r, decreases from 375 to 345 and the dielectric loss increases from 0.0161 to 0.0385 as the measuring frequency increasing from 100Hz to 100kHz. This reflects the dielectric relaxation characteristic of ferroelectric perovskit structure of PZT.

The PZT cantilever is actuated through the piezoelectric effect of d_{31}. To evaluate the actuation mechanism the piezoelectric constant d_{31} needs to be determined. There was no available means to measure d_{31} directly; so it was estimated with the following equation using measured data of d_{33} and e_{31}:

$$e_{31} = (c_{11} + c_{12})d_{31} + d_{33}c_{13}$$

Where, the e_{31} and d_{33} were measured using a piezometer, d_{33} and e_{31} can be calculated using the method outlined in [7], the $c_{11,}$ c_{12} and c_{13} are stiffness constants of PZT. After substituting the following data: e_{31}=0.8C/m, d_{33}=34pC/N, c_{11}=126GPa, c_{12}=79.5GPa and c_{13}= 84.1GPa, into above equation, a value of 14pC/N was obtained for d_{31}.

5. CONCLUSION

A reliable process to fabricate silicon cantilevers using SOI wafers that incorporating PZT actuating elements has been established. Previous cantilevers fabrication using SOI wafers has involved deep etching to the buried oxide layer. HF etching of the oxide layer was then used to release the cantilever. This is not possible when PZT is present as it is very difficult to protect PZT from the HF attack. To circumvent this deep etching was used to etch through silicon to the buried oxide from both sides of the wafer. The cantilevers were released by RIE of the buried oxide layer.

To provide sufficient piezoelectric actuation for the cantilever to act as a RF microswitch, the PZT should be at least 1μm tick. To ensure accurate pattern definitions of the PZT film a two-stage process, dry etching followed by wet etching, was used.

The PZT cantilevers were found to have little deformation upon release as a result of stress balancing between layers.

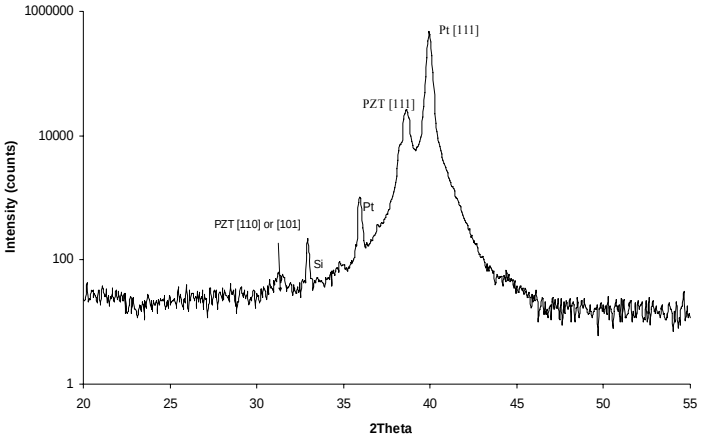

Figure 11: XRD examination on the crystallization of a five-layer PZT film (300nm)

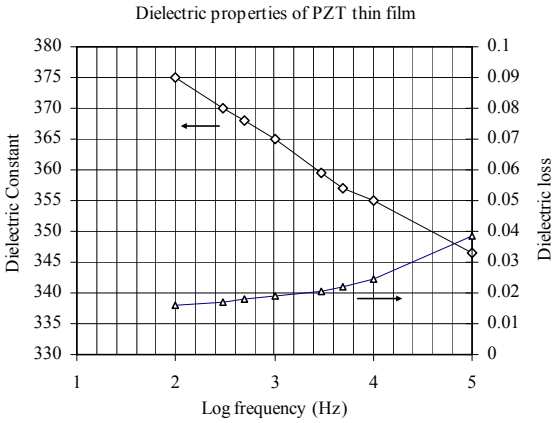

Figure 12: Dielectric properties of PZT

6. ACKNOWLEDGEMENTS

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